

ONS00317  
10/072,145

REMARKS

Claims 1-11 and 26-33 remain in the application. By this amendment, applicants have cancelled claims 12-25 without prejudice as to the subject matter contained therein.

By this amendment, claims 1, 5, 8, 9, 10, 11, 26, 28, and 33 have been amended. Applicants' specification including paragraph [0027] together with FIGS. 4 and 6 supports the changes to claims 1, 5, and 26. Paragraph [0019] supports the changes to claims 8, 9, and 33. Paragraph [0024] supports the changes to claims 10 and 11. Applicants have amended claim 28 to have proper antecedent basis with respect to its base claim 26.

Applicants believe that this amendment places the claims in better form for allowance or consideration on appeal, and respectfully request that Examiner Magee grant its admission.

A. Response to First 35 U.S.C. §103 Rejection

Claims 1, 2, 5, 6, 8-11, and 26-29 were rejected under 35 U.S.C. §103(a) as being obvious over Lur et al., USP 5,640,041 (hereinafter "Lur"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a semiconductor device that includes a semiconductor substrate having a surface formed with a first recessed region. A first dielectric material is deposited in the first recessed region and formed with a

ONS00317  
10/072,145

second recessed region having walls. A semiconductor layer is formed in proximity to the second recessed region, and a thermal oxide layer is formed integral with the semiconductor layer, wherein the thermal oxide layer seals the second recessed region while leaving a void in the second recessed region.

Applicants respectfully submit that Lur fails to make claim 1 obvious because Lur does not show or suggest, among other things, a semiconductor layer formed in proximity to the second recessed region, and a thermal oxide layer formed integral with the semiconductor layer. In Lur, there is no semiconductor layer shown or suggested at all, and Lur specifically uses a deposited oxide to seal his recessed regions. Lur's structure significantly reduces void volume as shown in Lur's FIG. 7, and degrades the resultant dielectric constant. For at least these reasons, applicants respectfully believe that claim 1 is allowable.

Claim 2 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 5 depends from claim 1 and further calls for the semiconductor layer to comprise polysilicon. Claim 5 is believed allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that claim 5 is allowable because Lur does not show or suggest a polysilicon layer as called for in claim 5.

Claims 6 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 8 depends from claim 1 and further calls for the first dielectric material to be recessed below a major surface of the semiconductor substrate. Claim 8 is believed allowable for at least the same reasons as claim 1. Additionally, applicants respectfully submit that claim

ONS00317  
10/072,145

8 is allowable over Lur because Lur does not show or suggest a first dielectric material recessed below a major surface of the semiconductor substrate.

Claim 9 depends from claim 8 and is believed allowable for at least the same reasons as claims 8 and 1.

Claim 10 now depends from claims 1 and 7 and further calls for a polysilicon layer deposited on walls of the second recessed region. Claim 10 is believed allowable for the same reasons as claim 1. Additionally, claim 10 is believed allowable because Lur does not show or suggest a polysilicon layer deposited on walls of the second recessed region.

Claim 11 depends from claims 1 and 7 and further calls for an amorphous silicon layer deposited on walls of the second recessed region. Claim 11 is believed allowable for the same reasons as claim 1. Additionally, claim 11 is believed allowable because Lur does not show or suggest an amorphous silicon layer deposited on walls of the second recessed region.

Claim 26 calls for a semiconductor device comprising a semiconductor substrate having a surface formed with a first recessed region. A first dielectric material is deposited in the first recessed region and formed with a second recessed region having an opening and walls. A semiconductor cap layer is formed adjacent the opening, and a thermal oxide layer is grown on the semiconductor layer to form a seal the opening.

Applicants respectfully submit that Lur fails to make claim 26 obvious because Lur does not show or suggest a semiconductor cap layer formed adjacent the opening. Additionally, Lur does not show or suggest a thermal oxide layer grown on the semiconductor layer to seal the opening.

ONS00317  
10/072,145

In Lur, there is no semiconductor cap layer shown or suggested adjacent an opening. Additionally, Lur specifically uses a deposited oxide for the second dielectric material, which fills the recess, and because of its poor step coverage, pinches off to form a seal. Lur's approach significantly reduces void volume as shown in Lur's FIG. 7, and degrades the resultant dielectric constant. For at least the above reasons, applicants respectfully believe that claim 26 is now allowable.

Claim 27 depends from claim 26 and further calls for the semiconductor cap layer to comprise polysilicon. Claim 27 is believed allowable for the same reasons as claim 26. Additionally, claim 27 is believe allowable because Lur does not show or suggest a polysilicon cap layer as recited in claim 27.

Claim 28 depends from claim 27 and is believed allowable for at least the same reasons as claim 27 and 26.

Claim 29 depends from claim 26 and is believed allowable for at least the same reasons as claim 26.

#### B. Response to Second 35 U.S.C. §103 Rejection

Claims 3, 4, 30 and 31 were rejected under 35 U.S.C. §103 over Lur in view of Zakeriya et al., US Pub. 2003/0030107 A1 (hereinafter "Zakeriya"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claims 3 and 4 depend from claim 1. Applicants respectfully submit that Zakeriya does not make up for the deficiencies of the Lur reference as described above in Section A, and that the combination of Lur and Zakeriya

ONS00317  
10/072,145

fails to make claim 1 obvious for the reasons stated above. Thus, applicants believe claims 3 and 4 are allowable for at least the same reasons as claim 1.

Claims 30 and 31 depend from claim 26. Applicants respectfully submit that Zakeriya does not make up for the deficiencies of the Lur reference as described above in Section A, and that the combination of Lur and Zakeriya fails to make claim 26 obvious for the reasons stated above. Thus, applicants believe claims 30 and 31 are allowable for at least the same reasons as claim 26.

C. Response to Third 35 U.S.C. §103 Rejection

Claims 7, 32 and 33 were rejected under 35 U.S.C. §103 over Lur in further view of Holbrook et al., USP 6,495,853 (hereinafter "Holbrook"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 7 depends from claim 1, and applicants respectfully submit that Holbrook does not make up for the deficiencies of the Lur reference as described above. Applicants further submit that the combination of Lur and Holbrook fails to make claim 1 obvious for the reasons stated above in Section A. Thus, applicants believe claim 7 is allowable for at least the same reasons as claim 1.

Claims 32 and 33 depend from claim 26. Applicants respectfully submit that Holbrook does not make up for the deficiencies of the Lur reference as described above in Section A, and that the combination of Lur and Holbrook fails to make claim 26 obvious for the reasons stated above. Thus, applicants believe claims 32 and 33 are allowable for at least the same reasons as claim 26.

ONS00317  
10/072,145

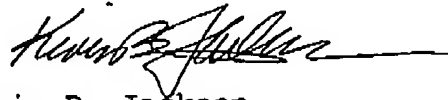
Conclusion

Applicants have made an earnest attempt to place the application in condition for allowance. In light of the above amendments and remarks, applicants respectfully request reconsideration and allowance of the pending claims.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite Examiner Magee to call the undersigned attorney at the Examiner's convenience.

Respectfully submitted,

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